implanted into a silicon substrate, through a gate oxide layer. The substrate is then annealed in a low temperature furnace, to form $Si_{1-x}Ge_x$ in the channel region.

PENDING ISSUE FOR RECONSIDERATION

Were claims 11, 13-14, 24-28, 30-32, and 38-43 properly rejected under 35 U.S.C. §103(a) as being unpatentable over Aronowitz (U.S. pat. No. 5,296,386) in view of Grider (U.S. Pat. No. 5,818,100)?

GROUPING OF CLAIMS

Although Applicant considers each pending claim to be separately patentable, and the claims do not stand or fall together, a detailed response to the pending rejections will emphasize independent claims 11, 24, 25, 28, 30, 38, 40, and 41.

ARGUMENT

§102 Rejection of the Claims

Claims 11, 24, 25, 30 and 32 were rejected under 35 USC §102(b) as anticipated by Aronowitz et al. (US 5,296,386).

Aronowitz appears to describe a $Si_{1-x}Ge_x$ channel region. However, Aronowitz does not show a length of its channel region.

In contrast, Applicants' independent claims as amended show a $Si_{1-x}Ge_x$ channel region having a channel length less than 7μm. Due to the state of technical knowledge as of the date of Applicant's invention, the recited length of the channel is a distinguishing and novel feature.

Because Aronowitz does not disclose all elements of Applicant's claimed invention, a 35 USC §102 rejection is not appropriate. Withdrawal of Examiner's rejection is therefore respectfully requested.

§103 Rejection of the Claims

Claims 11, 24, 25, 30 and 32 were rejected under 35 USC §103(a) as obvious over Aronowitz (US 5,296,386) in the alternative to Examiner's 35 USC §102(b) rejection.

As amended, Applicant contends that the element of a $Si_{1-x}Ge_x$ channel region having a channel length less than 7μm is not obvious as a matter of general knowledge in the art. Withdrawal of Examiner's §103(a) rejection over Aronowitz is therefore respectfully requested.

Applicant also anticipates Examiner's reintroduction of Grider (US 5,818,100) as a reference to support Examiner's previously argued position that Applicant's invention is obvious over Aronowitz in view of Grider.

The Examiner has the burden under 35 U.S.C. §103 to establish a *prima facie* case of obviousness. *In re Fine*, 5 U.S.P.Q. 2d 1596, 1598 (Fed. Cir. 1988). In combining prior art references to construct a *prima facie* case, the Examiner must show some objective teaching in the prior art or some knowledge generally available to one of ordinary skill in the art that would lead an individual to combine the relevant teaching of the references. *Id.* The M.P.E.P. contains explicit direction to the Examiner that agrees with the court in *In re Fine*:

> In order for the Examiner to establish a *prima facie* case of obviousness, three base criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a *reasonable expectation* of success. Finally, the prior art reference (or references when combined) must teach or suggest *all the claim limitations*. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. (Emphasis added)

M.P.E.P. § 2142 (citing *In re Vaeck*, 947 F.2d 488, 20 U.S.P.Q.2d (BNA) 1438 (Fed. Cir. 1991)).

Grider appears to disclose a transistor device with elevated $Si_{1-x}Ge_x$ source/drain regions. Grider appears to suggest that devices are possible with an "underlying channel length of 0.25 micrometers." (col. 1, lines 22-37). Grider, however, does not include, teach or suggest a **$Si_{1-x}Ge_x$** channel region having a channel length less than 7μm.

In contrast, Applicant's invention contains a $Si_{1-x}Ge_x$ channel region having a channel length less than 7μm. Applicant contends that this element is not contained, taught or suggested by Aronowitz or Grider independently or in combination and respectfully requests withdrawal of

Examiner's 35 U.S.C. §103 rejections with respect to independent claims 11, 24, 25, 28, 30, 38, 40, and 41.

There is no motivation from Grider to pursue channel length reduction in a $Si_{1-x}Ge_x$ channel region.

Applicants contend that Grider cannot properly be combined with Aronowitz to preclude patentablility of Applicants invention, because Grider only teaches manufacture of elevated source/drain regions. Grider does not teach manufacture of channel regions, and more significantly, Grider does not teach the manufacture of $Si_{1-x}Ge_x$ channel regions. Therefore, there is no teaching, suggestion or enablement, provided within Grider or in the knowledge generally available to one of ordinary skill in the art, to support the manufacture of a $\mathbf{Si_{1-x}Ge_x}$ channel region having a channel length less than 7μm. Grider does not even attempt to tackle the problem associated with forming a $\mathbf{Si_{1-x}Ge_x}$ channel region having a channel length less than 7μm adjacent to a gate oxide since Grider is only directed toward the manufacture of elevated source/drain regions which do not abut a gate oxide.

There is no reasonable expectation of success in Aronowitz or Grider

Aronowitz and Grider, either alone or in combination, do not provide a reasonable expectation of success to arrive at the present invention. A transistor with a $Si_{1-x}Ge_x$ channel region having a channel length less than 7μm did not exist prior to the Applicant's invention. Even more the same was not achievable. Consequently, even if one of ordinary skill desired to modify the teachings of Aronowitz and Grider, there is no expectation of success because such a structure could not be built. Therefore, there is no reasonable expectation of successfully constructing the present inventive structure based on Aronowitz and Grider at the time the present invention was made. Accordingly, the present invention patentably distinguishes over Aronowitz and Grider, either alone or in combination.

Moreover, obvious to try to make such a device to decrease the size of a $Si_{1-x}Ge_x$ channel transistor is insufficient to render the made structure obvious. And, obvious to try is not equivalent to actually make the claimed structure for the first time as the Applicant's claimed

invention does. A structure created for the first time is patentable. Previously, it was not possible to optimize beyond the parameters of the known capability in the prior art. Thus, apart from the novel method of forming, the structure so formed is itself novel and nonobvious.

The prior art references do not teach or suggest all of the claim limitations.

The Applicant acknowledges the Examiner's correctness in stating that the present case is to be examined on the basis of the structure itself. The Applicant's claimed transistor is a novel structure apart from its method of forming. The Examiner has not produced a single reference or a combination of references as part of his prima facie duty which possesses or suggests all of the claim limitations, e.g. the $Si_{1-x}Ge_x$ channel having a channel length less than 7μm, or shown any expectation of success for the same, as recited in independent claims 11, 24, 25, 28, 30, 38, 40, and 41.

The present disclosure teaches a method for constructing the structure of the present invention and the novel, claimed structure. Aronowitz and Grider do not teach how one of ordinary skill can construct the present invention. Specifically, Aronowitz and Grider do not teach how to make, or the structure per se, of a transistor which has a $Si_{1-x}Ge_x$ channel region having a channel length less than 7μm. Only by reading the present disclosure into Aronowitz and Grider can their teachings be modified to possibly arrive at the present invention. It is a well know tenet of patent law that hindsight reconstruction is prohibited.

Claims 13, 26, 27 and 31 were rejected under 35 USC §103(a) as being unpatentable over Aronowitz et al. (US 5,296,386) together with Crabbe' et al. (US 5,821,577). Claims 11, 14, 24, 25, 28, 30, 32, 38, 40 and 41 were rejected under 35 USC §103(a) as being unpatentable over Selvakumar et al. (US 5,426,069) together with Aronowitz (US 5,296,386). Claims 13, 26, 27, 31, 39, 42 and 43 were rejected under 35 USC §103(a) as being unpatentable over Selvakumar et al. (US 5,426,069) together with Aronowitz (US 5,296,386) and Crabbe' et al. (US 5,821,577).

Neither Crabbe' not Selvakumar cure the deficiencies of Aronowitz or Grider. Therefore Applicant's invention is not contained within the cited references individually or in combination. Applicant therefore respectfully requests withdrawal of Examiner's 35 USC §103(a) rejections

as to independent claims 11, 24, 25, 28, 30, 38, 40, 41, as well as all claims depending therefrom as dependent upon allowable claims.

Conclusion

Applicant respectfully submits that the claims are in condition for allowance and notification to that effect is earnestly requested. The Examiner is invited to telephone Applicant's attorney (612-373-6913) to facilitate prosecution of this application.

If necessary, please charge any additional fees or credit overpayment to Deposit Account No. 19-0743.

Respectfully submitted,

LEONARD FORBES

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Date 10/18/2000 By _____
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CERTIFICATE UNDER 37 CFR 1.8: The undersigned hereby certifies that this correspondence is being deposited with the United States Postal Service with sufficient postage as first class mail, in an envelope addressed to: Commissioner of Patents, Washington, D.C. 20231, on this 18 day of October, 2000.

Amy Moriarty
Name

Amy Moriarty
Signature